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OPTIMIZED SYSTEM LEVEL DESIGN AND SIMULATION ANALYSIS FOR CHARACTERIZATION OF PERFORMANCE OF SINGLE-LOOP CT SIGMA-DELTA MODULATORS A/D

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ABSTRACT

This paper demonstrates a possibility to realize a simulation of testing strategy of high-resolution Sigma-Delta modulator using MATLAB SIMULINK and Xilinx EDA tool environment. This brief works explore towards smart computation static and dynamic parameter of sigma delta Analog and converter (ADC) .Novelty of computation method introduce here in the Output Response Analyzer (ORA) and On chip test generation being used for testing of ADC parameters which help in reducing the difficulties in design complexity of integrated circuit . Moreover, the reusable features of hardware in the computation of different parameters are also improved in the ORA design of BIST.

KEYWORDS: Sigma delta modulator , Resolution, Noise Calculation, Power Calculation .

I. INTRODUCTION

Continuous time sigma delta modulator's are affected by the non ideal behaviour of analog circuit which limits their resolution in MHz bandwidth[1-2]. The non idealities of circuit and quantization noise constitute the modulator's noise floor. The error to be reduced or noise has its own power penalty depending on the Oversampling ratio (OSR) , quantizer bit length (Nc), the modulator's noise shaping order (Lc) , The share of each error in modulator's noise floor and OSR , Nc , Lc are the most important design parameters which will be responsible for minimizing the power consumption of a bandwidth and resolution[3-7] .To get the optimum loop filter coefficients and the amplifiers specifications are the objective of given system level design approach. The loop filter coefficients are optimized for the minimum quantization noise and the amplifiers specification are optimized for the minimum power consumption[8] . The task of testing a VLSI chip to guarantee its functionality is exceptionally complex and often very time taking. In addition to the difficulty of testing the chips (IC) themselves, the incorporation of the chips into systems has caused test generation's cost to grow highly. On the other hand, in built-in self-test, the test pattern generation and the output response evaluation are done on chip; thus, the use of high-end automatic test equipment (ATE) machines to test chips can be avoided[9-12]. High-resolution ADCs with high sampling rates are required in a broad area of high-performance applications, such as high-grade imaging systems, wireless communications, and radar[9]. To deliver ADCs satisfying the requirements of the applications, it is obligatory that they are tested as less time as possible, but without negotiating the quality of the test[11]. So with reduced size, cost and power consumption, the promotion towards the development of new generation of electronics system accomplishing all major features for the interaction of real time world to the digital processing circuitry is in its great demand[12][13].

A Successful system level modelling of sigma delta BIST for ADC linearity testing must satisfied following Condition: First ,it include modelling of TSG Test signal generator and post silicon implementation of TSG so that Low cost and Area overhead is minimize on chip and more accurate stimulus needed than ADC under test. Second System level Modelling and physical design of DUT as analog to digital converter play very important role[14-18]. Analog to digital linearity characteristics is mesuresued by two popular instruments such as INL and DNL. Integral nonlinearity(INL) and differential nonlinearity(DNL) can be calculated accurately from

estimation of ADC's transition levels. The most powerful approach to estimate transition level of ADC's is histogram test which gives solution of full code testing [19-23].

Noise parameter which affects the resolution of continuous time sigma delta modulator are:

- Thermal noise
- Clock jitter noise
- Quantization noise
- Limited gain bandwidth
- Slew rate of amplifiers

The errors which are mentioned above , can be reduced or eliminated by system or circuit level techniques carries a low part of modulator's noise floor (10-20%) . The calculations of Thermal noise and clock jitter noise have a more power reductions and they form usually (70-80)% of the modulator's noise floor[5-6]. This shows thermal noise and clock jitter noise mainly affects the modulator's noise floor. On the other hand , quantization noise contains (5-10%) of the modulator's noise floor[7-10].

II. Method: (GUI of Power Consumption)

The Power of countinuous time sigma delta modulator is estimated in terms of its system level parameters. we calculate separately the power budget of each modulator .

Figure 1. GUI of Power consumption .

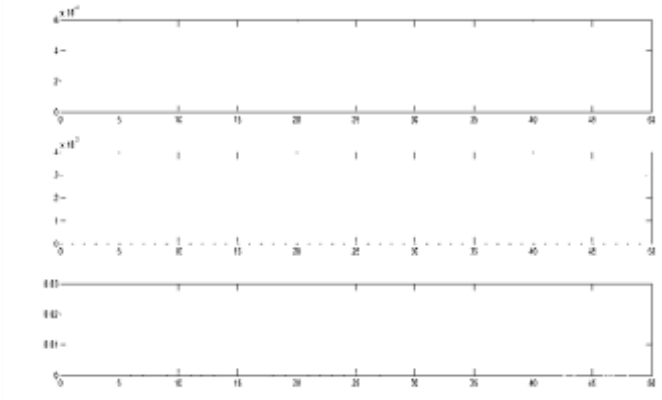

Figure 2. Power consumption Vs OSR.

As we have prepared a graphical user interface for the noise calculation presented in the secton II. Foe different values of all the parameters we are getting various values of noise parameters.

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Figure 3. GUI of Noise Calculation

III. RESULTS AND DISCUSSION

As we have prepared a graphical user interface for the noise calculation presented in the secton II. Foe different values of all the parameters we are getting various values of noise parameters .

Table 1 Noise Calculation Table

Ref	BW (MHz)	B(bit)	Lc	Nc	IBN_th	IBN_NRZ	IBN_q
[1]	18	8	3	4	0.113	0.24	2.7
[2]	20	8	3	4	0.240	0.42	3.1
[3]	25	16	3	5	0.340	0.48	3.2
[4]	36	16	4	1	0.140	0.36	3.4

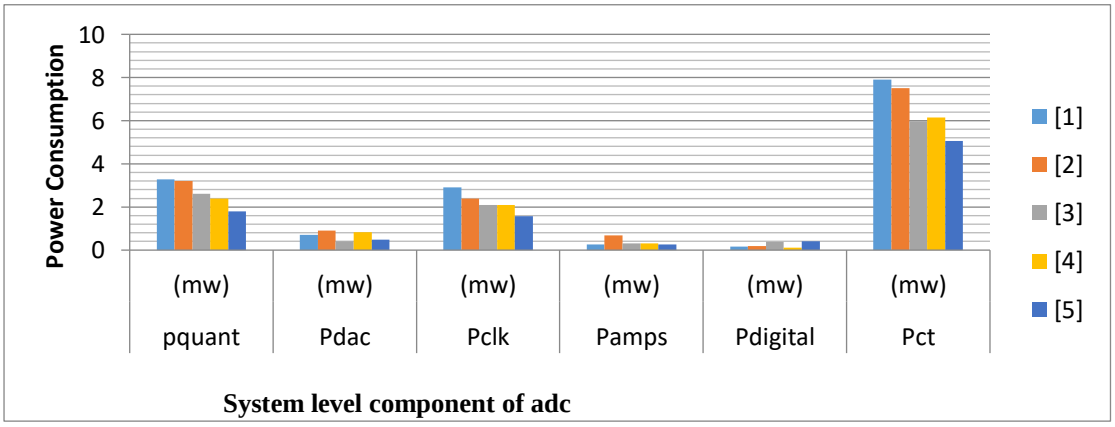

Figure 4. Comparative Noise Calculation

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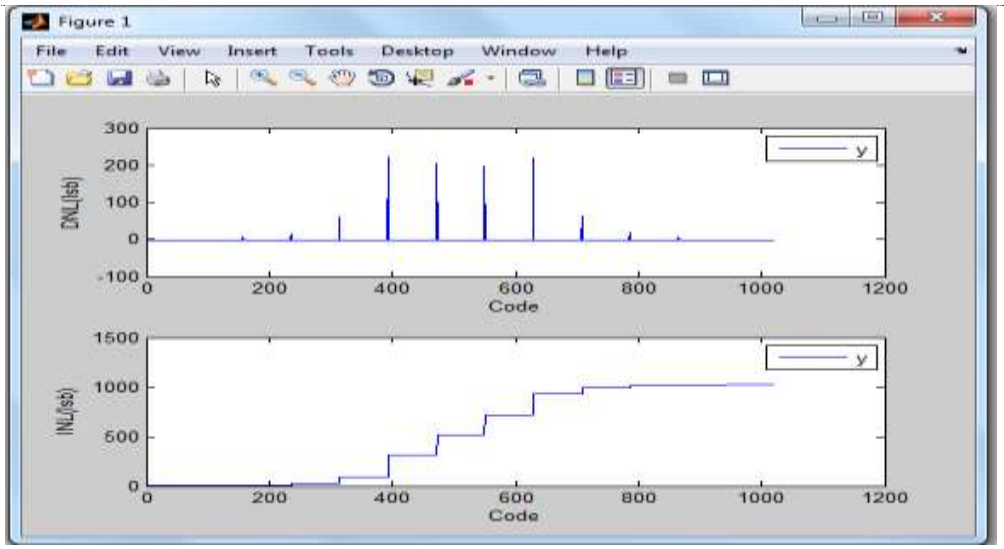

Figure 5. SIMSIDES Computation of INL and DNL

Histogram Calculator:DNL ,INL and SNRd is calculated using performing following equqtion(1),(2),(3).

$$DNL\left(K^{th}code\right)=\frac{W_k-1LSB}{1LSB} \quad (1)$$

$$INL\left(K^{th}code\right)=\sum_{i=0}^{i=k-1}\frac{W_i-KLSB}{1LSB} \quad (2)$$

$$SNR_d=-10\log\left(Error\right) \quad (3)$$

IV. CONCLUSION

In this paper noise parameters and power consumption in single stage sigma delta modulator are analytically extracted.The power consumption of different possible design of CT sigma delta modulator are compared to choose the best one. GUI allows us to get the power values without actually simulating the circuit design. Further , The transistor level design can be implemented and the author is free to use any tool for the designn. Here selected different values of OSR , Lc , Nc and various parameter and got different values of power and in recent results for Lc=3 , Nc=4 , B= 12 . Therefore, the accuracy of the proposed technology is considerably high. Since the proposed technology is entirely a digital circuit therefore, the performance of the modulator ORA will not be degraded. In addition, the obtained parameters are tested by using BIST technology. This worked us foused our system level Modeling and Post simulation strategy to obtain fast and accurate prototype of the ADC Built –In-self-test of sigma –delta based ADC. Our approach consist of modelling and design of an accurate first order sigma delta modulation based ADC.The synthesis result using a 180 nm library and MATLAB Simulink is used .

V. ACKNOWLEDGEMENTS

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